

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/98	Serial No. 10/561,135
	Applicant(s) VORBACH et al.	
	Filing Date April 25, 2006	Group Art Unit 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,151,611	April 24, 1979	Sugawara et al.			
	5,036,493	July 30, 1991	Nielsen			
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	1044571	February 16, 1989	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Ballagh et al., "Java Debug Hardware Models Using JBits," 8 th Reconfigurable Architectures Workshop, 2001, 8 pages.
	Bellows et al., "Designing Run-Time Reconfigurable Systems with JHDL," Journal of VLSI Signal Processing 28, Kluwer Academic Publishers, The Netherlands, 2001, pp. 29-45.
	Culler, D.E; Singh, J.P., "Parallel Computer Architecture," Page 17, 1999, Morgan Kaufmann, San Francisco, CA USA, XP002477559.
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	Price et al., "Debug of Reconfigurable Systems," Xilinx, Inc., San Jose, CA, Proceedings of SPIE, 2000, pp. 181-187.
	Short, Kenneth L., Microprocessors and Programmed Logic, Prentice Hall, Inc., New Jersey 1981, p. 34.
	Sundararajan et al., "Testing FPGA Devices Using JBits," Proc. MAPLD 2001, Maryland, USA, Katz (ed.), NASA, CA, 8 pages.
	Webster's Ninth New Collegiate Dictionary, Merriam-Webster, Inc., 1990, page 332 (definition of "dedicated").

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.